

QUALIFICATION AND RELIABILITY FOR MEMS AND IC PACKAGES

Reza Ghaffarian, Ph.D.

Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA

Reza.Ghaffarian@JPL.NASA.Gov, (818) 354-2059

ABSTRACT

Advanced IC electronic packages are moving toward miniaturization from two key different approaches, front- and back-end processes, each with their own challenges. Successful use of more of the back-end process front-end, e.g. microelectromechanical systems (MEMS) Wafer Level Package (WLP), enable reducing size and cost. Use of direct flip chip die is the most efficient approach if and when the issues of know good die and board/assembly are resolved. Wafer level package solve the issue of known good die by enabling package test, but it has its own limitation, e.g., the I/O limitation, additional cost, and reliability. From the back-end approach, system-in-a-package (SIAP/SIP) development is a response to an increasing demand for package and die integration of different functions into one unit to reduce size and cost and improve functionality.

MEMS add another challenging dimension to electronic packaging since they include moving mechanical elements. Conventional qualification and reliability need to be modified and expanded in most cases in order to detect new unknown failures. This paper will review four standards that already released or being developed that specifically address the issues on qualification and reliability of assembled packages. Exposures to thermal cycles, monotonic bend test, mechanical shock and drop are covered in these specifications. Finally, mechanical and thermal cycle qualification data generated for MEMS accelerometer will be presented. The MEMS was an element of an inertial measurement unit (IMU) qualified for NASA Mars Exploration Rovers (MERs), Spirit and Opportunity that successfully is currently roving the Martian surface.

Key words: Thermal cycle, solder joint, area array package, reliability, MEMS, microelectromechanical systems, inertial measurement unit, MER

INTRODUCTION

IC Package Technology Trend

BGAs and CSPs (chip scale package) are now widely used for many electronic applications including portable and telecommunication products. System-in-a-package (SIP) development is the most recent response to further increasing demand for integration of different functions into one unit to reduce size and cost and improve functionality.

The BGA version has now widely started to be implemented for high reliability applications with unique requirements. The BGA version of the area array package, introduced in late '80's and implemented with great caution in early '90's was further evolved in the mid '90's to the CSP, also called fine pitch BGA, with a much finer pitch to 0.4mm. Now, distinguishing between size and pitches become difficult for the array versions.

These are all now categorized as area array packages in order to be able to distinguish them from the flip chip bare die category. Bare dies have been around for a longer time, but their associated issues- including known good die and difficulty in direct attachment to printed wiring boards (PWB)- have limited their wide implementation. Wafer level packages introduced several years ago to address the key issues of bare die and take the advantage of package ease of testing and handling. As PWB technology with finer features become widely available with lower cost, bare die become more attractive.

Extensive work has been performed by the JPL consortia in understanding technology implementation and reliability issues in transitioning from BGAs to CSPs. Lessons learned by the team have been continuously published and presented in previous SMTAI conferences¹⁻². The books published also include chapters related on these subjects and lead-free solder alloy defects³⁻⁶.

Recent approaches in IC packaging have been to increase functionality through SIP technology, i.e., stacking dice/packages in order to avoid reducing the array pitch. This approach will ease stringent board and assembly requirements. The first SIP used CSPs and included two stacks of flash and SRAM die in a single package. Also known as multi-chip package (MCP), it has now been recently released in four-die format and may include two flash memories, a fast-cycle-RAM (FCRAM), and an SRAM. Figure 1 shows schematically a number of SIP/stack package technologies including combination of die and package stacks. It includes a schematic drawing of a unique silicon based SIP package⁷ that was developed using discrete flip chip die attached to a microboard with area array configuration.

The stack die packages are moving toward developing more than six die within a package using extremely thin die⁸ in order to meet the package total height requirement. A

supplier of semiconductor assembly and test service announced in early 2004 shipment of a 6 die stack chip scale package in a thin, 1.6-mm profile. This dime-sized 3D package, 17x17 mm, has more than 400 leads, and houses a DSP or an applications-specific IC (ASIC) chip, along with flash and SDRAM. Its market is compact foot-print products such as cell phones, personal digital assistants (PDAs), and digital camera applications. Japanese companies have recently introduced a 9-die stack packages for similar applications.

MEMS Technologies

In the United States, the technology is known as microelectromechanical systems (MEMS), in Europe as microsystems technology (MST), and in Japan as Micromachines. MEMS are integrated micro devices or systems combining electrical, mechanical, fluidic, optical, (and all physical domains) components fabricated using integrated circuit (IC) compatible batch-processing techniques and range in size from micrometers to millimeters^{9, 10}.

MEMS devices include microscopic machines such as valves, pumps, switches, and actuators. MEMS are unique in that they perform both mechanical and electrical functions, and physically move. MEMS both harvest data and issue commands based on the data. A MEMS with a miniature tuning fork, for instance, can gather information about the direction of sound waves, which can prompt a command to shift the position of a microphone for better sound quality.

MEMS are built similar to integrated circuits. They are fabricated on silicon wafers by patterning various layers of materials and releasing (under-etching). After release, these tiny structures are capable of motion. If the microstructure is a mirror, and the device can move and manage light, the device can be considered an optical MEMS, also known as a MOEMS.

Some of the MEMS technology has been around for years as summarized in Table 1. Computer printer heads, automotive air bag actuators, brake sensors and engine heat sensors are examples of MEMS devices found today. Analog Devices' ADXL line of air-bag accelerometers and Texas Instruments' Digital Micromirror Device (DMD) display technology are commercial success stories. MEMS devices have traditionally been used to gather ambient data like temperature or pressure, but are expanding into more complex uses that involve optoelectronics and biotechnology. For example, MEMS devices can be used in new drug testing in the pharmaceutical industry, or in blood-screening sensors that can perform complete tests at bedside.

New switches including RF and relay versions are now being built by MEM process to replace traditional switches such as waveguide and conventional solid-state RF technologies such as PIN diodes¹⁰. Current solid-state RF

technologies (PIN diode- and FET- based) are utilized for their high switching speeds, commercial availability, low cost, and ruggedness. Their inherited technology maturity ensures a broad base of expertise across the industry, spanning device design, fabrication, packaging, applications/system insertion and, consequently, high reliability and well-characterized performance assurance.

In spite of this design flexibility, two major areas of concern with solid-state switches persist: breakdown of linearity and frequency bandwidth upper limits. Above 1-2 GHz frequencies, this technology shows fundamental degradation in insertion loss and isolation. RF MEMS switches using various microfabrication techniques will bring significant improvement with lower power consumption.

The MEM switches combine the advantages of traditional electromechanical switches (low insertion loss, high isolation, extremely high linearity) with those of solid-state switches (low power consumption, low mass, long lifetime). Because of high package cost, the MEMS switch application currently will be limited to aerospace, defense, and unique commercial applications until a low-cost production and packaging methods have been established.

Currently, MEMS/MOEMS tend to be custom built, and assembled on batch production lines. Standards do not exist for MEMS, particularly. This coupled with the fact that little sharing of information on MEMS, makes MEMS sort of a mysterious device. However, there is a great deal of interest in MEMS - and optoelectronic packages - which puts these packages in the same league as CSPs a few years ago.

QUALIFICATION SPECIFICATION FOR ASSEMBLY RELIABILITY

An industry-wide guideline document, IPC SM785, for accelerated reliability testing of solder attachment has been around for more than a decade. Only recently, industry agreed to release an industry-wide specification, IPC9701, in response to BGA and CSP technology implementation⁶. The IPC SM785 guideline, although very valuable and still valid, did not answer the key question of what the data means in terms of product application and data comparison. As is well established by industry and the JPL Consortia¹⁻⁵, many variables could be manipulated to either show favor or disfavor test results.

Also, in some cases, considerable resources and time could be wasted to generate failure data not related to solder attachment. An example is the use of a surface finish having the potential of inducing intermetallic rather than solder joint failure. This is especially likely for a novice user/supplier.

The IPC 9701 specification, addresses how thermal expansion mismatch between the package and the PWB

affects solder joint reliability. In order to be able to compare solder joint reliability for different package technologies, PWB materials (e.g., FR-4), using a relatively thick nominal control thickness to minimize bending (0.093”), surface finish choice to eliminate intermetallic failure (OSP, HASL), pad configuration to eliminate failure due to stress riser (non solder mask defined), and pad size to have a realistic failure opportunity for package/PWB (80%-100 package pad), etc. were standardized in order to minimize their effect on the test results.

Since the release of this document in early 2002, there has been questions regarding why other variables (including use of immersion Au/Ni surface finish) are realistic production finish for many product applications is not allowed in this specification. Potential technical issues associated with the use of such variables were the key elements that the team decided not to include them in the specification. It should be noted, however, that package suppliers/users can evaluate this surface finish or others (or any other variables) as they become available, as long as deviations from the specification are clearly stated.

The thermal cycle (TC) test ranges, test profile, and the number of cycles (NTC) reported were also standardized. These include the reference cycle in the range of 0 to 100° C (TC1) and a severe military cycle condition of -55 to 125°C (TC4). Three out of five total TC conditions are identical to the test conditions recommended by JEDEC 22 Method A104, Revision A. The NTC varied from a minimum value of 200 cycles to a reference value of 6,000 cycles.

The IPC committee is currently working on the A revision of this specification to include requirements for the lead-free solder alloy attachment. Two key areas of concerns are the

current dwell time that may not be sufficient for lead-free solder creep occurrence, currently defined 10 minutes for lead contained solder, and the surface finish that is not compatible with lead-free-solder requirement.

The IPC reliability committee continued to work on follow on specifications including performance test methods and requirements for damage induced by mechanical and dynamic loading.

IPC-JEDEC 9702 released in July 2004, establishes common method of characterizing the fracture resistance of board-level device interconnects to flexural loading during non-cycling board assembly and operation. Monotonic bend test qualification pass/fail requirements need to be mutually agreed between the customer and supplier.

IPC 9703 currently being developed addresses the dynamic performance by providing specific mechanical shock test procedures, increasing shock level till failure, and failure analyses approaches. It also addresses unique shock and drop requirements based on the established current industry standards and available information. Again, failure data could be utilized to answer requirement that are mutually agreed between customer and supplier.

IPC 9704 describes specific requirements for strain gage testing Printed Wiring Board (PWB) and system assembly. This procedure enables board manufacturers to conduct required strain gage testing independently. Also, it could be used as guideline for strain gage attachment required for IPC 9702 and other specifications.

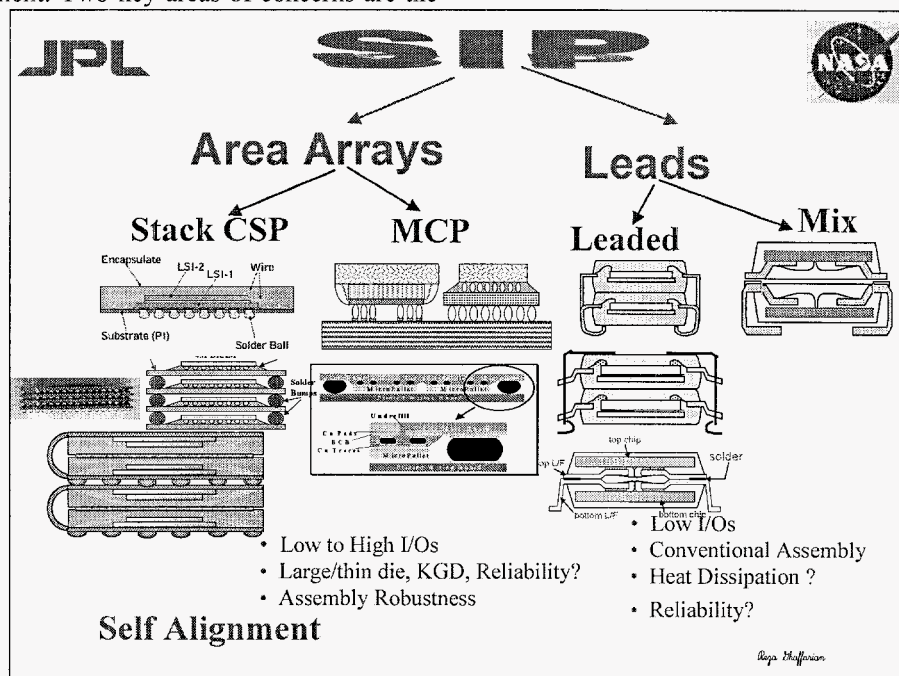



Figure 1 Categories of SIP package technology, both leaded and area array packages

Table 1 MEMS development and implementation within the last few decades

| <div>  </div> | | | | |
|--|-----------|-------------------|----------------|------------------------|
| Product | Discovery | Product Evolution | Cost Reduction | Full Commercialization |
| Pressure Sensors | 1954-1960 | 1960-1975 | 1975-1990 | 1990 |
| Accelerometers | 1974-1985 | 1985-1990 | 1990-1998 | 1998 |
| Nozzles | 1972-1984 | 1984-1990 | 1990-1996 | 1996 |
| Photonics/displays | 1980-1986 | 1986-1998 | 1998-2004 | 2004 |
| Bio/Chemical Sensors | 1980-1994 | 1994-2000 | 2000-2004 | 2004 |
| Radio Frequency (R.F.) | 1994-1998 | 1998-2001 | 2001-2005 | 2005 |
| Gyros/Rate Sensors | 1982-1990 | 1990-1996 | 1996-2002 | 2002 |
| Micro Relays | 1977-1982 | 1993-1998 | 1998-2002 | 2002 |
| Pressure Sensors: Ford, Honeywell, Lucas Novasensor, Sensym Accelerometer: Analog Devices, Motorola, Nippondenso, and SensorNor | | | | |
| Source: Grace Associate Rupa Bhaffian | | | | |

MEMS ACCELEROMETER QUALIFICATION

Mars Exploration spacecraft and Rovers (MERs) were equipped with a high reliability commercial-off-the-shelf (COTS) inertial measurement units (IMUs). The IMUs sense acceleration using MEMS and angular motion and convert them to outputs that are used by vehicle control systems for guidance. One IMU is mounted on the backshell, or heat shield, of the spacecraft's entry vehicle, while another is installed in the rover. Both units maintain spacecraft attitude information and measure deceleration during descent into the Martian atmosphere to help determine when a parachute can be deployed safely to slow the spacecraft during entry. The rover IMU provides attitude and acceleration information during surface operations, and positions the rover's high-gain antennae.

One IMU with 3 MEMS accelerometers were subjected to a number of qualification test including vibration, pyroshock, and thermal cycling to establish their reliability and implement modification in collaboration with supplier when is needed. Pyroshock requirement of 2000 g was severe; it required some modification to shock isolator in order to reduce stresses induced on some ncased electronics.

Thermal cycles in the range of -54°C to 71°C with power on/off were performed to simulate environmental exposure. The thermal cycle ranges were relatively benign to Mars surface temperature climate since the IMU was installed in warm electronic box with heater in order to reduce thermal extreme exposure. During testing, continuous monitoring

was performed to check the health of IMU. Test was stopped after 220 cycles, defined base on meeting 3 X mission life cycles, to perform visual inspection of the IMU unit. One MEMS accelerometer within IMU, then, was subjected to destructive physical analysis (DPA). Wire bond Results of DPA were compared to a virgin sample to determine if degradation occurred. Test results are presented.

Thermal Cycle

The following thermal cycle profile as schematically shown in Figure 2 were used for the IMU qualification.

1. The IMU was powered on at the start of each transition from cold (-54°C) to hot ($+71^{\circ}\text{C}$) and during hot dwell.
2. The IMU was powered off at the start of the transition from hot ($+71^{\circ}\text{C}$) to cold (-54°C) and during cold dwell.

DPA

After completion of 220 cycles, no anomaly was detected. One out of 3 MEMS accelerometer package was delided and inspected visually and by scanning electron microscopy to determine integrity of microstructure. Wire bonds were subjected to pull test and test results before and after were compared. Results were:

- Table 1 lists test results of wirebond pull tests. Out of 220 wirebonds that subject to pull test, one was lifted from the bond pad of the small diode to which it was

bonded, although it passed the Specified DPA bond pull requirement at 3.0 grams force. Subsequent analysis of this failure found the diodes aluminum bond pad to be contaminated with an extremely thick layer of aluminum oxide. Due to this contaminant the majority of the gold wirebond failed to form an intermetallic bond with the aluminum bond pad.

- Die shear test were performed on 17 dies, each of the two devices. All passed the Specified Minimum Required (2X) die shear requirements.

- A total of 34 passive elements were tested for shear force in each of the two devices. All passed the Specified Minimum Required (1X) shear requirements.

Examples of SEM Photomicrographs are shown in Figures 3-10.

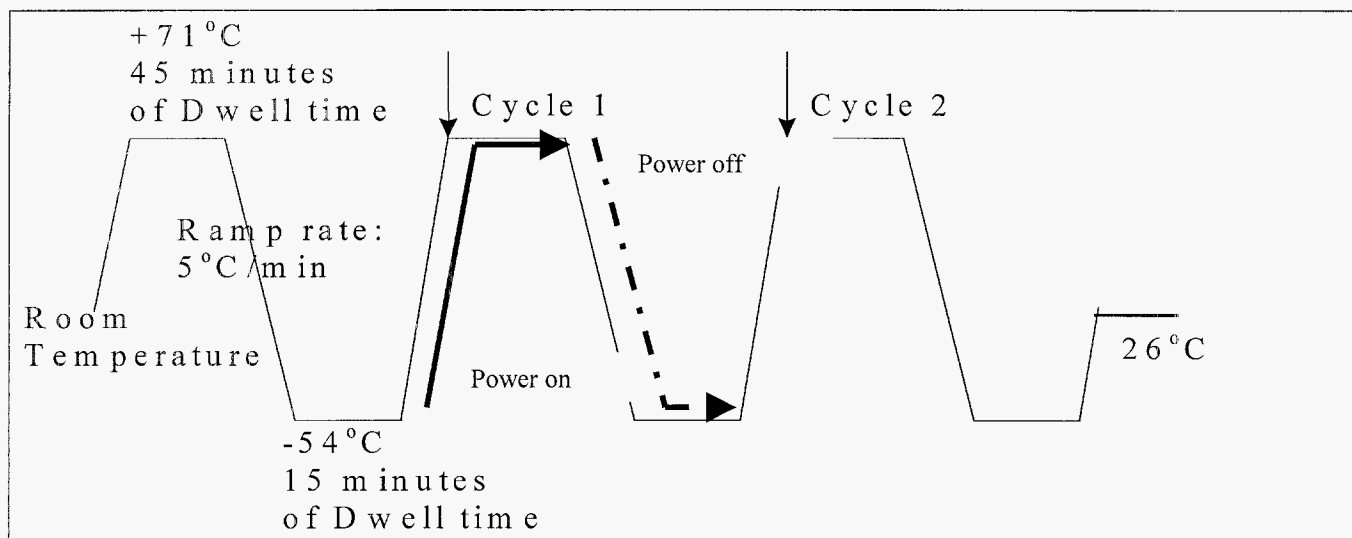


Figure 2 Thermal cycle profile for accelerometer

Table 2 Wire bond pull test of MEMS accelerometer

| Wire Material | Wire Diameter | Minimum Required Pull Strength | # Wires Pulled | Average Pull Strength | Minimum Pull Strength | Maximum Pull Strength |
|---------------|---------------|--------------------------------|----------------|-----------------------|-----------------------|-----------------------|
| Gold | 1.0 | 2.5 grams | 221 | 8.8 grams | 3.0 grams | 15.6 grams |

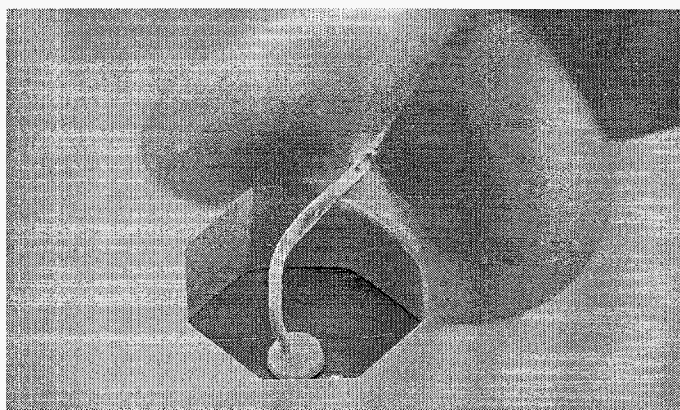


Figure 3 80X SEM photo showing the wirebond to the top of the device.

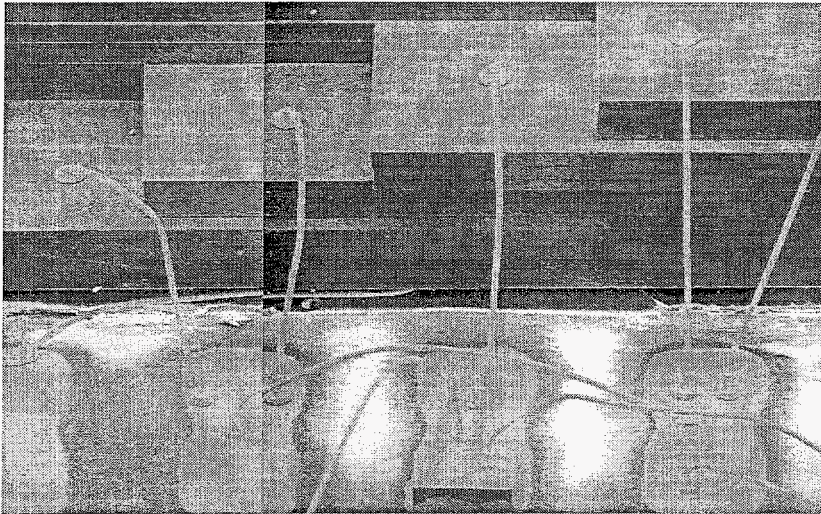


Figure 4 30X SEM view showing wirebonds that cross over adjacent substrate bond pads. This is allowable per MIL-STD-883 METHOD 2017.7

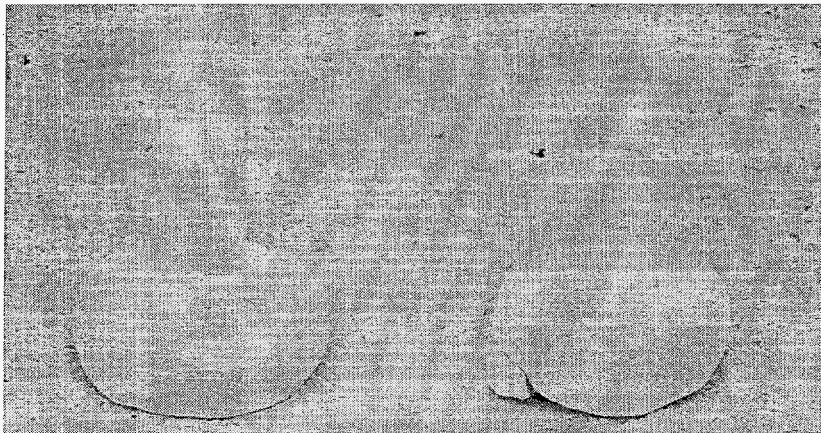


Figure 5 300X SEM view of the wirebonding method used to bond the wires from the accelerometer to the substrate bond pads. This is allowable per MIL-STD-883 METHOD 2017.7

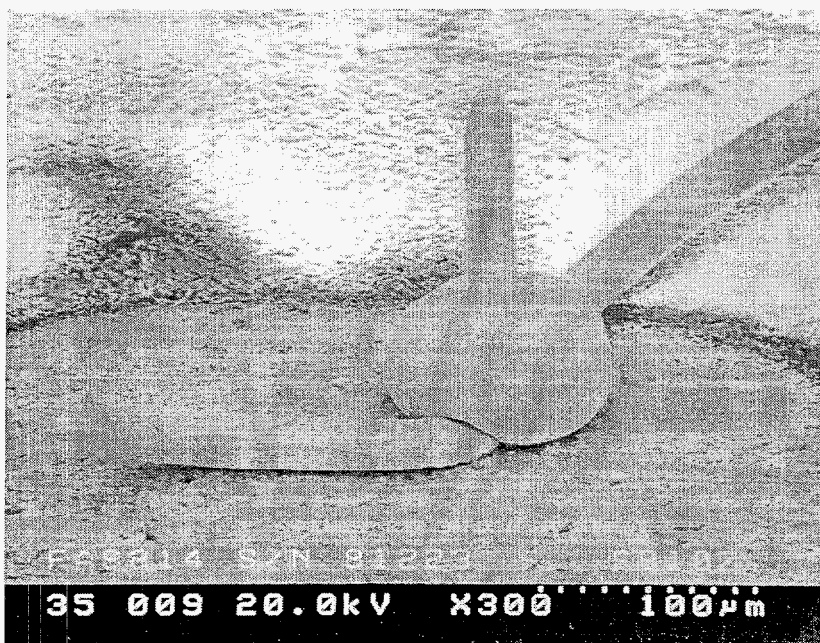


Figure 6 300X SEM view of an accelerometer wire to pad bond.

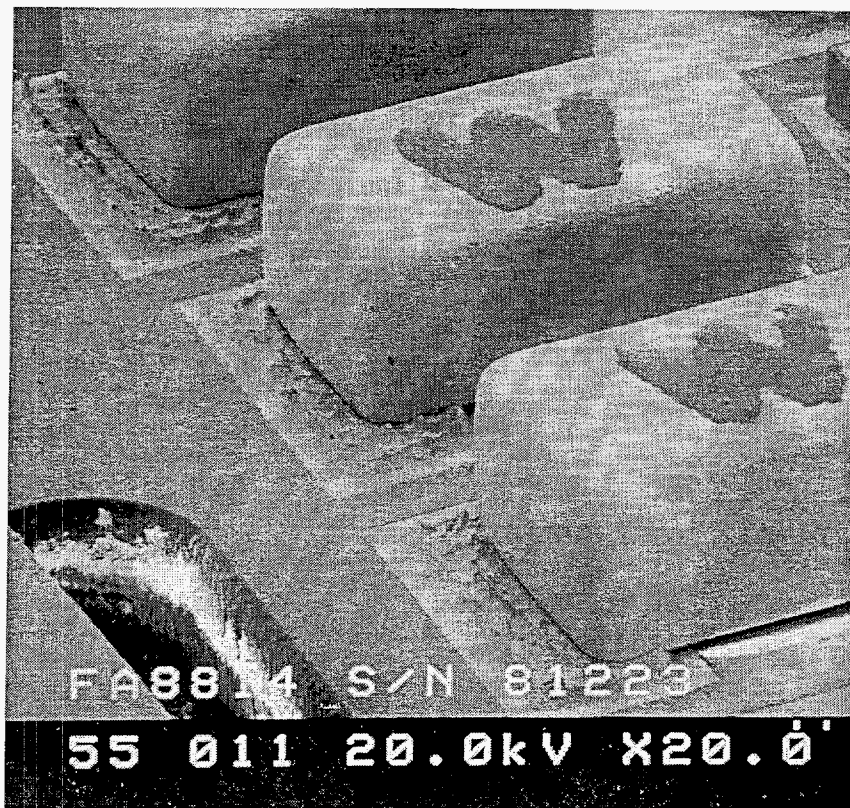


Figure 7 20X SEM view of silver/epoxy, passive component and die attach.

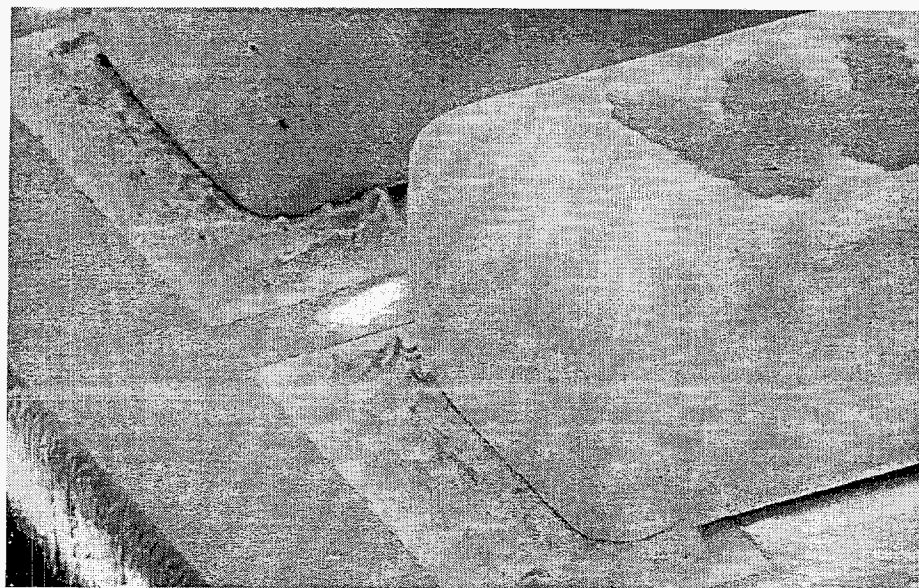


Figure 8 40X SEM view of silver/epoxy capacitor attach.

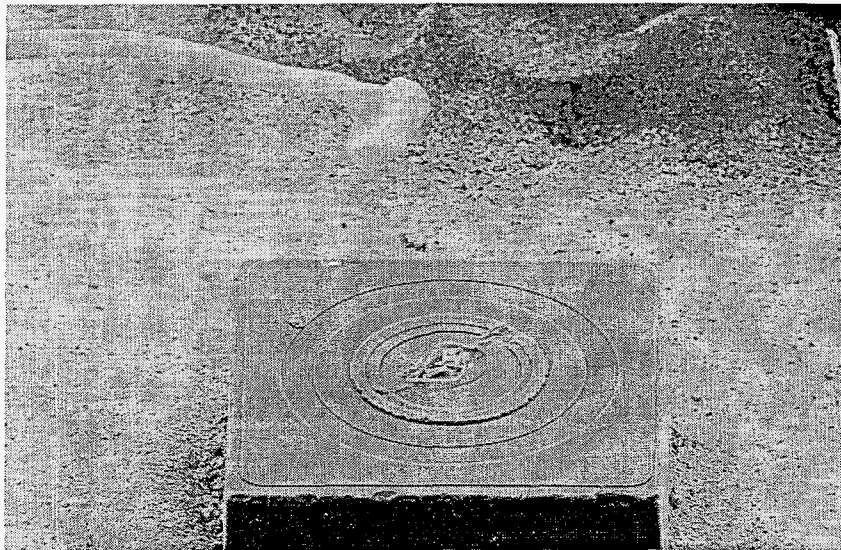


Figure 9 150X SEM photo of the wirebond lifted

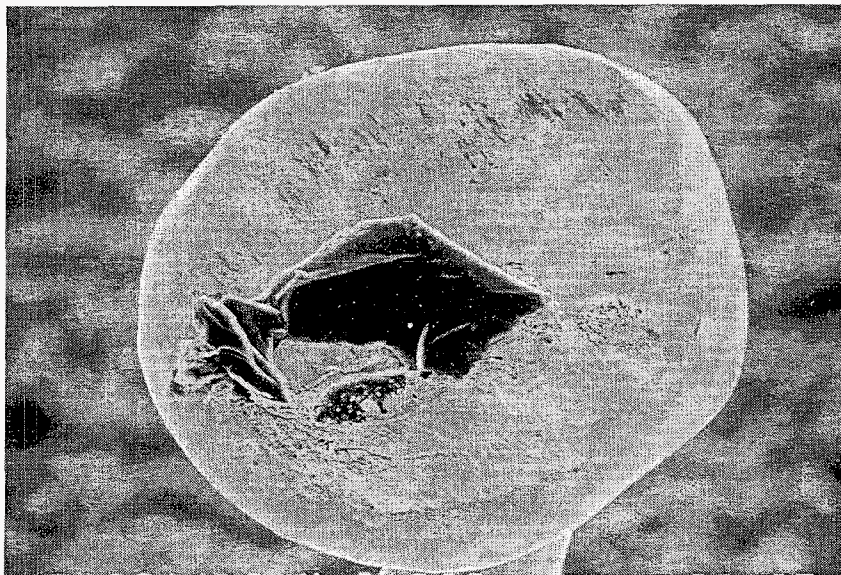


Figure 10 900X SEM photo of the bottom of the gold ball bond. Note there has been little to no inter metallic formation on the majority of the bond surface.

SUMMARY

As electronic packages become smaller and more complex, sophisticated modeling and testing as well as probability risk assessment based on failure data may be required for their effective implementation. Current industry specifications are released or being developed to address both thermal cycle and mechanical loading requirements. Four IPC specifications developed under reliability committee, 6-10d, to address such requirements are: IPC 9701, IPC-JEDEC 9702, IPC 9703, and IPC 9704.

MEMS Accelerometers, as a part of an IMU package, were inspected for manufacturing workmanship and then subjected to thermal cycle and vibration/shock tests to characterize their behavior and determine their failure

mechanisms. MEMS accelerometer subjected to 220 cycles in the range of -54°C to 71°C , with power on at hot and off at cold dwells. The IMU showed no signs of degradation during thermal cycle test continuously monitored electrically and an accelerometer was subjected to destructive evaluation for wirebonds, die, and passive shear tests. No degradation due to thermal and environmental exposures was observed.

ACKNOWLEDGEMENTS

The research described in this publication is being carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration.

The author extends his appreciation to the IPC 6-10d technical committee and Edward Litty, MER IMU Project Lead. Special thanks to Sid Johnson, Ken Evan, and Dr. Ramesham at JPL for providing SEM, DPA, and thermal cycle test support. Sincere thanks to program managers at NASA Electronic Parts and Packaging Program (NEPP) including Dr. Charles Barnes and Phillip Zulueta for their continuous support and encouragement.

REFERENCES

1. Ghaffarian, R., Kim, N., Rose, D., Hunter, B., Devitt, K., Long, T., "*Rapid Qualification of CSP Assemblies By Increase of Ramp Rates and Cycling Temperature Ranges*", The Proceedings of Surface Mount International, Chicago, Sept. 30-Oct 4, 2001
2. Ghaffarian, R., Nelson, G., Cooper, M., Lam, D., Strudler, S., Umdekar, A., Selk, K., Bjorndahl, B., Duprey, R., "*Thermal Cycling Test Results of CSP and RF Package Assemblies*", The Proceedings of Surface Mount International, Chicago, Sept. 25-28, 2000
3. Fjellstad, J., Ghaffarian, R., Kim, YG., *Chip Scale Packaging for Modern Electronics* (Electrochemical Publications, 2002)
4. Ghaffarian, R., "Chip Scale Package Assembly Reliability", Chapter 23rd in *Area Array Interconnect Handbook* (Kluwer Academic Publishers, edited by Karl Puttlitz, Paul Totta, 2002)
5. Ghaffarian, R., "BGA Assembly Reliability", Chapter 20, *Area Array Packaging Handbook* (McGraw-Hill Publisher, Ken Gilleo, Editor)
6. Ghaffarian, R., "Characterization and Failure Analyses of Lead-Free Solder Alloy Defects", Chapter 16, *Lead-Free Solder Interconnect Reliability* (to be published by ASM International, Dogkai Shangguan, Editor)
7. Goetz, M.P., "Thermal Mechanical Stress Analysis of a Silicon-based System-in-a-Package", *Solid State Technology*, July 2000
8. Greathouse, S., "Systems in Package Technology at Intel", Presented at SEMICON West, July 2004
9. Gardner, J., Varadan, V., Awadelkarim, O., *Microsensors, MEMS, and Smart Devices*, John Wiley & Sons, Ltd, 2001
10. Ramesham, R., Ghaffarian, R., Ayazi, F., "Fundamentals of Microelectromechanical Systems," Chapter 14, *Microsystems Packaging Book* by Rao Tummala, McGraw-Hill, 2001, ISBN0-07-137169-9
11. Wellman, J. "RF MEMS TRO", NASA Electronics Parts and Packaging (NEPP Document), <http://www.NEPP.nasa.gov>, Jan 2003
12. IPC 9701, "Performance Test Methods and Qualification Requirements for Surface Mount Solder Attachments". Published by IPC, Association Connecting Electronics Industries